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13. ABSTRACT *(Maximum 200 words)*

The purpose of this program was to demonstrate the capabilities of NDR devices for the design and fabrication of high-functionality for the design and fabrication of high-functionality digital circuits. Several basic circuit functions have been demonstrated using RTD-HBT devices and extensive software for CAD of various types of circuits including adders, correlators and multivalued logic circuits was developed and employed to estimate power/speed tradeoffs in various logic circuits.

Several Resonant Tunneling devices were fabricated including RTD's, RHETs, Esaki diodes and others. These diodes were then employed to demonstrate various logic functions such as AND, XNOR, Flip Flops and others. A Monolithic RTBT circuit to demonstrate a minority gate was also fabricated and demonstrated.

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FINAL PROGRESS REPORT

G. I. HADDAD AND P. MAZUMDER

1/31/97

U. S. ARMY RESEARCH OFFICE

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S. Mohan, J. P. Sun, P. Mazumder, G. I. Haddad, "Device and Circuit Simulation of Quantum Electronic Devices", *IEEE Trans. on CAD*, **14**, 653-662, 1995.

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S. Mohan, W. L. Chen, P. Mazumder and G. I. Haddad, "Bistable Mode Low Power Circuits Using RTDs and HBTs", *IEEE J. of Solid-State Circuits*, submitted, 1995.

H. L. E. Chan, S. Mohan, P. Mazumder, W. L. Chen and G. I. Haddad, "Ultrafast Compact Multiple-Valued Multiplexers Using Quantum Electronic Devices", presented at the GOMAC, San Diego, CA, November, 1994.

P. Mazumder, J. P. Sun, S. Mohan and G. I. Haddad, "DC and Transient Simulation of Resonant Tunneling Devices in NDR-SPICE", presented at the 21st International Symposium on Compound Semiconductors, 1994 (IOP Press).

S. Mohan, P. Mazumder and G. I. Haddad, "Circuit Simulation of Resonant Tunneling Devices Using NDR-SPICE," presented at IEDM, San Francisco, CA, December, 1994.

X. Wang, W. L. Chen, G. O. Munns, J. R. East and G. I. Haddad, "Comparative Study on Resonant Tunneling Diodes (RTD's) and Traditional Tunnel Diodes (TD's) and Their Co-Integration w ith Hetorjunction Bipolar Transistors (HBT's), presented at the 1995 International Semiconductor Device Research Conference, December 5-8, 1995, Charlottesville, Virginia.

S. Kulkarni, P. Mazumder and G. I. Haddad, "A 32-bit Ultrafast Parallel Correlator Using Resonant Tunneling Devices", presented at the International Conference on Integrated Micro-Nanotechnology for Space Applications, Houston, TX, October, 1995.

W. L. Chen, G. O. Munns, X. Wang and G. I. Haddad, "Co-Integration of High Speed Heterojunction Bipolar Transistors (HBTs) and Tunnel Diodes", presented at the 1995 IEEE/Cornell Conference on Advanced Concepts in High Speed Semiconductor Devices and Circuits, Ithaca, NY, August, 1995.

S. Kulkarni, P. Mazumder and G. I. Haddad, "A High-Speed 32-bit Parallel Correlator for Spread Spectrum Communication", presented at the Ninth International Conference on VLSI Design.

A. F. Gonzales and P. Mazumder, "Ultra-fast Adder Circuit Design Using Resonant Tunneling Diodes and Mosfets", presented at the Government Microcircuit Applications Conference, 1997.

8. SCIENTIFIC PERSONNEL SUPPORTED BY THIS PROJECT AND DEGREES AWARDED DURING THIS REPORTING PERIOD:

1. H. E. Chan, GSRA (June 1993 - May 1994)
2. M. Bhattacharya, GSRA (August 1994 - December 1996)
3. S. Mohan, GSRA, graduated with a Ph.D., 1994 (June 1993 - December 1994)
4. W. L. Chen, GSRA, graduated with a Ph.D., 1993 (June 1993 - December 1993)
5. A. F. Gonzalez, GSRA (January 1995 - December 1996)
6. X. Wang, GSRA (September, 1994-April, 1997)
7. G. Munns, Research Investigator, graduated with a Ph.D., 1997
8. J. East, Research Scientist

9. REPORT OF INVENTIONS: NONE

STATEMENT OF THE PROBLEM:

To demonstrate the capabilities of NDR devices for the design and fabrication of high-functionality digital circuits with special emphasis on multivalued logic and multistate memories.

SUMMARY OF RESULTS:

1. Fabrication of RTDs and RHETs: We have fabricated RTDs and demonstrated basic logic circuits such as AND, XOR and flipflops, as well as 3-state memories and C-elements. We have fabricated RHETs with InGaAsP graded collector barriers to achieve $\alpha = 0.98$ and PVR = 50, and f_T = 60GHz at 300K. We have built XNOR and flipflop circuits using RHETs.

2. Fabrication of BSRTTs: We have fabricated BSRTTs with ultrathin base layers (60 Å), ß = 3 and dß= 9 at 77K. Both room temperature and 80K transistor action were realized in the BSRTTs.

3. RTBT Fabrication: InP-based RTBTs with InGaAsP collector layers were investigated systematically for the first time. The fabricated RTBT consists of an AlAs/$In_{0.75}Ga_{0.25}As$/AlAs RTD structure in conjunction with a conventional InGaAs/InGaAsP HBT structure and the average DC current gain is 20. The low V_P and high current density (10^4 A/cm^2) make this RTBT attractive for high-speed applications. We have also built an XNOR gate and a frequency multiplier using RTBTs.

4. Tunnel Diode Fabrication: We have investigated tunnel diode structures consisting of InGaAs pn junctions grown on InP substrates. These first structures had current densities of 67 KA/cm^2 and an estimated speed index of 40. These types of performance numbers would be very useful as an alternative to RTDs if they could be easily fabricated.

5. Fabrication of RTD-HBT Integrated Logic: InP-based RTDs and HBTs have been integrated to build self-latching logic gates. NOR, NAND and inverted MAJORITY functions have been demonstrated in integrated form. The HBTs have ß = 200 and f_T = 60 GHz at 300K, while the RTDs have peak-to-valley ratios of 10-25 at 300K.

6. Development of NDR-SPICE: Previously incorporated models for RTDs and RTTs were evaluated on the basis of user-feedback from circuit designers. The model for the multiple peak RTD was improved to include state information essential to simulation. Earlier models for multiple peak RTDs based on the simple one-peak RTD were shown to be inadequate and impossible to use in complex circuit simulations involving transient analysis. The new MRTD

model considers the device to be a system with memory, unlike earlier models which just replicated the I-V characteristics. This enables the new model to accurately simulate the observed transient characteristics of 4-peak RTDs. Convergence problems associated with the new model were identified and solved. RTD, HBT, and MODFET models from Texas Instruments and other companies were incorporated into the NDR-SPICE simulator and used to design several self-latching and multiple-valued logic circuits. The accuracy of the simulator was initially verified by assembling several of these circuits using discrete components and comparing the simulated outputs with the observed outputs. The simulator was demonstrated at the International Electron Devices Meeting, 1994, San Francisco, and has evoked keen interest from several potential users. A delay estimator has been added to the simulator to project realistic performance of NDR circuits in the presence of layout artifacts such as interconnect parasitics.

7. Design of Novel Digital Circuits using RTDs, RHETs and other Devices: In the area of circuit design and simulation, several innovative circuits have been designed and simulated to reveal the intrinsic advantages of these devices with folded I-V characteristics that have been exploited carefully to design bistable-mode nanopipelined circuits for various digital functions (e.g., 32-bit addition, 32-bit parallel correlation, 32-bit parallel multiplication, ATM buffering, etc.). Self-latching logic was designed using RTDs and HBTs. These circuits are similar to the bistable RTT circuits in function but have better noise margins and promise higher operating speeds with current-mode operation. Optimization techniques for circuit design using RTDs and HBTs have been identified and used in the design of a few circuits. These optimization techniques allow the designer to choose the best values of parameters such as device area, noise margins of various kinds and operating voltages, given one or more constraints in terms of supply voltages, peak and valley voltages or currents, and so on. Circuits were also designed using RTDs and depletion-mode MODFET models supplied by Texas Instruments. NAND, NOR and inverted MAJORITY gates were designed and simulated. These designs were then transferred to Texas Instruments who performed the layout design and IC fabrication. Current-mode, bistable circuits with less than 0.5mW/gate dissipation up to 5 GHz were designed using RTDs and HBTs. These circuits include NAND, NOR and inverted MAJORITY gates. After initial validation of the design using the NDR-SPICE simulator and discrete assemblies, the circuits were fabricated in monolithic integrated form. Successful operation of all three circuit functions was demonstrated.

8. Design of Multi-state Memories using MRTDs and HBTs: Optimization criteria and design techniques for multi-state memories were developed. Given the number of memory states for a

particular circuit, constraints on peak and valley voltages and currents are obtained if certain noise and other margins are to be met. Conversely, if the device parameters are completely specified, operating voltages and currents are determined to maximize the noise margins on the lines and in the memory circuit itself. This can help to reduce the probability of a random noise spike causing the stored data to be corrupted.

9. Design of Multiple-valued Logic Circuits: Several basic multiple-valued logic circuits including multiplexers/demultiplexers, literal gates, counters and T-gates were designed using RHETs, RTBTs or a combination of RTDs and HBTs. These circuits were simulated using NDR-SPICE and some were assembled on a bread-board with discrete devices. A signed digit full adder using RTDs in conjunction with MOS devices has been demonstrated. The device characteristics of RTDs facilitate compact implementation of redundant signed digit systems thus greatly improving performance of arithmetic circuits such as adders and multipliers. Larger multivalued circuits have also been designed using RTDs such as a 16-bit signed digit fully parallel adder, 24x24 redundant binary adder tree multiplier, and a multivalued gate-arrays.

10. Theoretical Framework for RTD-based Circuits: Formal circuit analysis of NDR circuits built using HBTs and RTDs has been performed to determine power dissipation, noise margins, switching characteristics of basic gates in static and dynamic conditions. We have identified RTD and HBT device parameters that need to be optimized to obtain good performance from designed circuits in terms of high speed operation, low power consumption, and low voltage operation. Keeping in mind that ideal device characteristics desired for the best circuit design are not physically achievable at the present time, we have identified allowable tolerances in device characteristics that will still result in reliable operation of fabricated circuits.

INDUSTRIAL INTERACTION:

1. The University of Michigan research group has collaborated with Dr. Alan Seabaugh's group of researchers at Texas Instruments, Dallas on various aspects of NDR circuit design and simulation. We designed a 1-bit full adder using TI's Depletion-type MODFET and 3-Peak RTD devices and comprehensively simulated a nanopipelined series-parallel mode 32-bit adder circuit. TI has prepared the mask of several constituent circuit components, namely, majority gate, 2- and 3-input NOR gates, inverters, and they were fabricated at TI, Dallas. Subsequently, after testing these constituent blocks to verify high-speed operation, a complete nanopipelined adder is being

fabricated to demonstrate the advantages of tunneling devices over conventional CMOS and other technologies.

2. The University of Michigan has interacted with Lockheed-Martin in the design and fabrication of multipeak RTDs and also in seeking suitable applications of these devices in multivalued logic and memory circuits. Using the NDR-SPICE simulator developed at the University of Michigan, several multivalued circuits, e.g., 4-valued Mux/Demux, 4-valued Up/Down Counter, Literals, etc., have been designed and comprehensively simulated using Lockheed-Martin device models to demonstrate possible applications of these devices.

3. The University of Michigan has collaborated with Hughes Research Laboratory at Malibu to design and fabricate HBT and RTD based GHz logic circuits leading up to the potential fabrication of a 8-bit parallel correlator circuit.